PIO - Base Address: 0x1000.0600

GPIO23_00_DIR: Programmed I/O Direction (offset: 0x24)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIODIR[23:0]	Program I/O Pin Direction These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers.	24'b0

GPIO23_00_POL: Programmed I/O Pin Polarity (offset: 0x28)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIOPOL[23:0]	Program I/O Pin Polarity These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at any PIO pin, the corresponding bit should be set to '1'; a value of '0' will not modify the pin data. Note: The polarity controls affect both input and output modes.	24'b0

GPIO23_00_DATA: Programmed I/O Data (offset: 0x20)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/W	PIODATA[23:0]	Data Pin for Program I/O These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	24'b0

GPIO23_00_SET: Set PIO Data Bit (offset: 0x2C)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOSET[23:0]	These bits are used for setting bits in the PIODATA output register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

GPIO23_00_RESET: Clear PIO Data bit (offset: 0x30)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIORESET[23:0]	These bits are used for clearing bits in the PIODATA output register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

GPIO23_00_TOG: Toggle PIO Data bit (offset: 0x34)

Bits	Type	Name	Description	Initial value
31:24	-	-	Reserved	8'b0
23:0	R/C	PIOTOG[23:0]	These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect.	24'b0

SYSCTL - Base Address: 0x1000.0000

GPIOMODE: GPIO Purpose Select (offset: 0x60)

Bits	Type	Name	Description	Initial value
31:10	-	-	Reserved	24'b0
9	R/W	RGMII_GPIO_ MODE	0:Normal Mode 1:GPIO Mode Control GPIO[51:40]	1'b1
8	RW	SDRAM_GPIO_ MODE	0:Normal Mode 1:GPIO Mode Control GPIO[39:24]	1'b1
7	R/W	MDIO_GPIO_MODE	0:Normal Mode 1:GPIO Mode Control GPIO[23:22]	1'b1
6	R/W	JTAG_GPIO_MODE	0:Normal Mode 1:GPIO Mode Control GPIO[21:17]	1'b0
5	R/W	UARTL_GPIO_ MODE	0:Normal Mode 1:GPIO Mode Control GPIO[16:15]	1'b1
4:2	R/W	UARTF_ SHARE_MODE	UARF Full interface is shared with PCM, REFCLK, I2S, GPIO [14:7]. The detailed UARTF Mode Pin Sharing is shown in previous session.	3'b111
1	R/W	SPI_GPIO_MODE	0:Normal Mode 1:GPIO Mode Control GPIO[6:3]	1'b1
0	R/W	I2C_GPIO_MODE	0:Normal Mode 1:GPIO Mode Control GPIO[2:1]	1'b1

SPI_GPIO_MODE description

Pin Name	SPI_GPIO_MODE=0	SPI_GPIO_MODE=1
SPI_DIN	SPI_DIN	GPIO6
SPI_DOUT	SPI_DOUT	GPIO5
SPI_CLK	SPI_CLK	GPIO4
SPI_EN	SPI_EN	GPIO3

I2C_GPIO_MODE description

Pin Name	I2C_gpio_mode=0	I2C_gpio_mode=1
I2C_SCLK	I2C_SCLK	GPIO2
I2C_SD	I2C_SD	GPIO1

JTAG_GPIO_MODE description

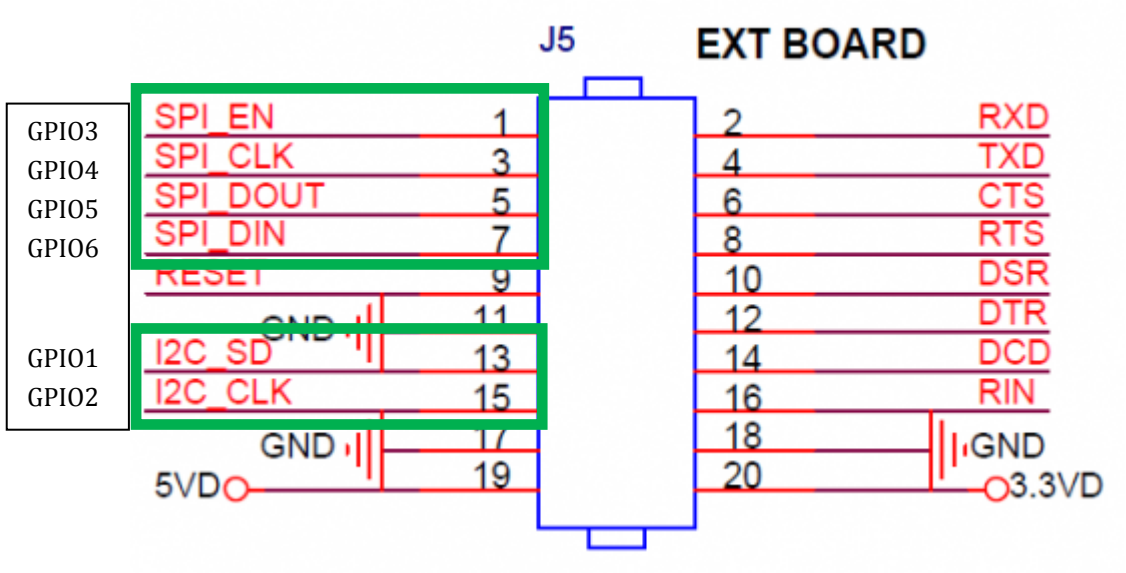
Pin Name	JTAG_GPIO_MODE=0	JTAG_GPIO_MODE=1
JTAG_TRST_N	JTAG_TRST_N	GPIO21
JTAG_TCLK	JTAG_TCLK	GPIO20
JTAG_TMS	JTAG_TMS	GPIO19
JTAG_TDI	JTAG_TDI	GPIO18
JTAG_TDO	JTAG_TDO	GPIO17

UARTL_GPIO_MODE description

Pin Name	UARTL_GPIO_MODE=0	UARTL_GPIO_MODE=1
RXD2	RXD2	GPIO16
TXD2	TXD2	GPIO15

UARTF_SHARE_MODE description

Pin Name	3'b000 UARTF	3'b001 PCM, UARTF	3'b010 PCM, I2S	3'b011 I2S UARTF	3'b100 PCM, GPIO	3'b101 GPIO, UARTF	3'b110 GPIO I2S	3'b111 GPIO
RIN	RIN	PCMDTX	PCMDTX	RXD	PCMDTX	GPIO14	GPIO14	GPIO14
DSR_N	DSR_N	PCMDRX	PCMDRX	CTS_N	PCMDRX	GPIO13	GPIO13	GPIO13
DCD_N	DCD_N	PCMCLK	PCMCLK	TXD	PCMCLK	GPIO12	GPIO12	GPIO12
DTR_N	DTR_N	PCMFS	PCMFS	RTS_N	PCMFS	GPIO11	GPIO11	GPIO11
RXD	RXD	RXD	REFCLK	REFCLK	REFCLK	RXD	REFCLK	GPIO10
CTS_N	CTS_N	CTS_N	I2SSD	I2SSD	GPIO9	CTS_N	I2SSD	GPIO9
TXD	TXD	TXD	I2SWS	I2SWS	GPIO8	TXD	I2SWS	GPIO8
RTS_N	RTS_N	RTS_N	I2SCLK	I2SCLK	GPIO7	RTS_N	I2SCLK	GPIO7



Notes :

1. All given GPIOs are 4mA drive capable.
2. The default direction for GPIO pins are input(i.e. tri-state) except the GPIO pins (GPIO17...GPIO21) shared with the JTAG interface. The default value for JTAG_GPIO_MODE is 1.